IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/699,756
Inventors	: Sun et al.
Filed	: November 3, 2003
TC/A.U.	: 2186
Examiner	: PATEL, HETUL B.
Docket No.	: P900384
Customer No.	: 33197
Confirmation No.	: 4258

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

SUPPLEMENTAL RESPONSE
AND EXAMINER INTERVIEW SUMMARY

Dear Sir:

This is in further response to the Final Office Action of December 26, 2007 issued by the United States Patent and Trademark Office regarding the above-identified application. A response to the Final Office Action is due three months from the mailing date thereof. Accordingly, this Response is being filed with a request for a one month extension of time. Applicants submit with this Response the following remarks and a Declaration Under 37 C.F.R. 1.131. Please kindly refer to and consider the following remarks and the attached document.

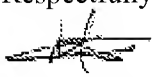
Claims 1-17 are currently pending in this application. Applicants respectfully request reconsideration in light of the following remarks.

Regarding the current prior-art rejections, Applicants submit herewith a Declaration under 37 C.F.R. 1.131, establishing that the invention by Applicants of the presently claimed patent application occurred before the relevant priority date of the Ikeda et al. patent. Accordingly, the Ikeda et al. reference does not appear to qualify as prior art under 35 U.S.C. 102(e), since it is not a patent granted on an application for patent by another filed in the United States before the invention by the Applicants for patent.

Multiple Examiner Interviews were conducted on March 25, 2008 with the Examiner of record, and were further conducted with his Supervisor. As a consequence of these discussions, it was agreed by the Examiner of record, having opened the file and more carefully reviewed the earlier-submitted Rule 1.131 Declaration, that all of the rejections would appear to have already been overcome with the earlier submission of that declaration. It was suggested by the Examiner's Supervisor, however, that the attached declaration, which contains more specificity, be submitted in order to buttress the strength of the Applicants' position. Accordingly, in light of the above items, reconsideration and withdrawal of all outstanding rejections is respectfully requested. Applicants respectfully submit that Claims 1-17, as currently presented, are in condition for allowance.

The Commissioner is hereby authorized to charge any needed fees to deposit account 50-1600.

Respectfully submitted,



Dated: March 27, 2008

Kenton R. Mullins
Attorney for Applicants
Registration No. 36,331

STOUT, UXA, BUYAN & MULLINS, LLP
4 Venture, Suite 300
Irvine, CA 92618
Tel: 949-450-1750
Fax: 949-450-1764

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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DECLARATION UNDER 37 C.F.R. 1.131

I, Albert Sun, Eric Sheu, and Shih-Liang Chen, declare as follows:

I am an inventor of the claims of the above-identified patent application.

Prior to May 24, 2002, I conceived the invention to a level of detail ready for patenting, as evidenced, for example, by pages 3-5 and 7-9 of the attached Exhibit, of an integrated circuit comprising an input port by which data is received from a source external to the integrated circuit; a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;

memory storing instructions for a mission function for the integrated circuit, and storing instructions for an initialization function used to transfer the configuration data to the programmable configuration points within the configurable logic array in response to an initialization event; and a processor coupled to the memory which fetches and executes said instructions from the memory, as described and claimed in the above-identified application.

The attached Exhibit illustrating my invention was prepared by me before May 24, 2002. The Exhibit document was subsequently transmitted to HAYNES BEFFEL & WOLFELD, LLP for preparation and filing of an application for patent in the United States.

The below undersigned declares that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, being duly warned that willful false statements and the like are punishable by fine or imprisonment, or both, (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing therefrom.

MAR 26 2008 — Albert Sun

Date — Albert Sun

MAR 26 2008 — Eric Hsu

Date — Eric Sheu

MAR 26 2008 — Shih-Liang Chen

Date — Shih-Liang Chen

INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

代撰編號：_____

提案編號：_____

□自撰□代撰:【Mark】(請填入事務所)

Title of this invention (本發明名稱)	
中　文	嵌入式可程式邏輯元件之電路重置架構
English	In-Circuit Configuration Architecture for embedded Programmable Logic Device

Content (目錄)

1. Inventors Information (發明人基本資料)
2. **Summary of the technical characteristics about this invention.**
   (簡述本發明之技術重點)
3. **Comparing prior patents or other prior arts with this invention.**
   (本發明與專利前案或其他先前技術(非專利)之比較)
4. Brief describing the best mode embodiment of this invention. (詳述本發明之最佳實施例)
5. Describing any possible modification or variation of this invention.
   (說明本發明任何可能之變化或修改)
6. Describing how the invention achieves the objects of the invention.
   (說明本發明的元件或步驟特點，何以達到發明目的)
7. Drafting the protective scope of the invention (claims) using the essential elements or steps of the invention.
   (試以最少必要元件或步驟，研擬本發明之保護範圍，注意請勿使用「單句式」)
8. Showing related drawings or experimental data about this invention.
   (示出本發明相關之圖式或實驗數據。註：此並非申請專利之絕對必要。)
9. Witnesses Information (見證人資料)

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

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INVENTION DISCLOSURE FORM

代撰編號：_____
提案編號：_____

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

1. Inventor (發明人) (請依貢獻比例順序填寫)							
Chinese Name (中文姓名)	ID No. (身分證號碼)	Citizenship (國籍)	Department (部門)	Ext. No. (分機)	Contribution (貢獻比例%)	Signature (簽名)	Date
	English Name (英譯姓名/同護照)	Address (中/英文地址並列)					
孫駿恭	F101926929	US	ED500	5520	35%		
	Albert Sun	新竹市湖濱二路 37 號 3 樓 3 F, No. 37, Waterfront Road II, Science-Based Industrial Park, Hsunchu.					
許志銘	R121054343	TW	NA	NA	35%		
	Eric Sheu	新竹市科學園區研新 3 路 3 號 No. 3, Creation Road III, Science-Based Industrial Park, Hsunchu.					
陳世梁	M121479579	TW	ED500	5587	30%		
	Shih-Liang Chen	豐原市三村路 122 巷 3 號 No. 3, 122 Lane, San-tsun Road, Fengyuan					

Remark :1. The inventors should have a substantial contribution to the idea of this invention. The inventor should propose or make a modification at least one element on this invention. One merely offering a consultation, experimentation, operation, or auxiliary work is not qualified.
(具發明人資格者，應為對本發明特徵範圍之「構想」具有實質貢獻者，發明人至少須提出或改良本發明一項構件以上，單純的諮詢、實驗、操作、或輔助工作等，不能列為發明人)

2. In order to preserve Macronix's right to patent this invention, descriptions of your invention should be treated as MXIC confidential. This invention should only be disclosed to non-Macronix employees under a approved and executed Non-Disclosure Agreement (NDA).
(為確保旺宏申請專利之權利，本發明之內容應屬機密，未經允許或簽訂保密合約(NDA)者，不得揭示於任何非相關人員或非旺宏員工)

3. Any publication, disclosure without an NDA, sale of this invention prior to file a patent application will be deemed as the prior art of this invention and make this invention devoid of novelty or a granted patent invalid.
(在本發明提出專利申請之前的任何公開、未經 NDA 之發表、上市銷售、或相關產品文件之散佈，都會被視為本發明之先前技藝，而使本發明喪失新穎性，並有可能使獲准之專利無效)

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

本資料為旺宏電子股份有限公司智慧財產及機密，非經書面許可不得以任何方式翻製或複印。

2. Summary of the technical characteristics about this invention. (簡述本發明之技術重點)

In-circuit configuration for embedded programmable logic device (PLD) is important for SOC era.

This invention describe how to implement in-circuit configuration for embedded programmable logic device on a chip.

The elements of this invention include configuration handler (stored in ROM or Flash), micro controller, PLD control circuitry, configuration data memory (RAM or Flash) and programmable logic device.

Through the above elements, the in-circuit configuration for embedded PLD could be achieved.

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INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

3. Comparing prior arts with this invention. (本發明與先前技術之比較)

Describing summary and disadvantages of each prior *Patents* or other prior arts *(Besides Patent)*, and comparing with this invention.

(簡述各專利前案或其他先前技術(非專利)之缺點及其與本發明之比較)

Remark: In the course of patent application, the inventor must submit any acknowledged prior art or related disclosures. Otherwise, a granted patent may be canceled. (依美國專利法之規定，在專利申請過程中，發明人必須陳報任何已知之前案或相關資料。否則，獲准之專利有可能會被取消)

Patent No or Prior arts (專利號或先前技術名稱)	Summary and advantages of prior patents or other prior arts (專利前案或其他先前技術之簡述及其缺點)	Difference from this invention (與本發明之差異)
5901330	**An architecture for an integrated circuit with in-circuit programming Include a micro controller on an integrated circuit and one or more banks of non-volatile memory which store instructions, including an in-circuit programming(ICP) set of instructions.**	**1. Integrated configuration data memory (RAM or Flash) on a chip.** **2. Configuration for PLD could be controlled by control circuitry.** **3. During initial power-up, configuration data in RAM or Flash will be configured into PLD automatically through control circuitry.** **4. Configuration data memory could be programmed or written using configuration handler, micro controller, control circuitry.** **5. All elements for embedded PLD configuration are on a chip.**

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

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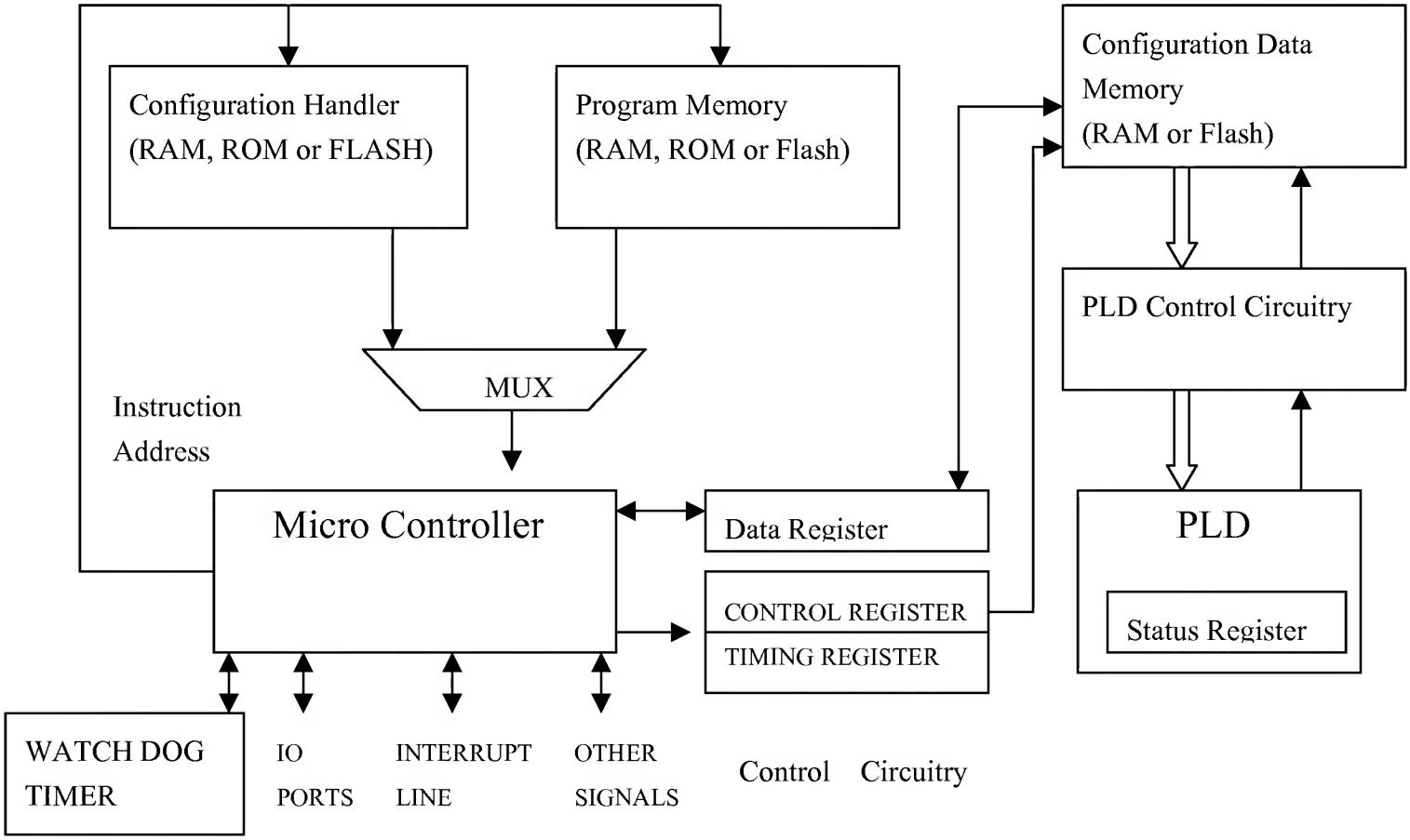
INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

4. Brief describing the best mode embodiment of this invention. (詳述本發明最佳實施例)

(若為 1.電子案：須作電路元件、方塊圖、電路原理之說明；2.若涉及軟體：須提供軟體流程及相關說明；3.若為機構案：須描繪其個別元件、組合圖，並作裝置動作、效果說明；4.若為製程案：須作對應於流程之剖面圖及其說明)



（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

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INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

5. Describing any possible modification or variation of this invention.
(說明本發明任何可能之變化或修正)

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

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INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

6. Describing how the invention achieves the objects of the invention.
(說明本發明何以達到發明目的)

1. **Integrated configuration data memory (RAM or Flash) on a chip**

2. **Configuration for embedded PLD could be controlled by control circuitry.**

3. **During initial power-up, configuration data in RAM or Flash will be configured into PLD automatically through control circuitry.**

4. **Configuration data memory could be programmed using configuration handler, micro controller, control circuitry.**

5. **All elements for embedded PLD configuration are on a chip.**

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

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7. Drafting the protective scope of the invention (claims) using the essential elements or steps of the invention. (試以最少必要元件或步驟之原則，研擬本發明之保護範圍)

An apparatus for in-circuit programming of an integrated circuit, comprising :

A processor on the integrated circuit which executes instructions;

An external port on the integrated circuit through which data is received from an external source;

A first memory array on the integrated circuit, which stores instructions for execution by the processor, including a set of instructions for controlling the transfer of instructions into the integrated circuit from the external source through the external port and instructions for execution by the processor, including a set of instructions for controlling the in-circuit programming steps of erasing, programming and verifying the data in programmable logic device.

A second memory array on the integrated circuit, which stores configuration data for programmable logic device.

A programmable logic device for a configurable integrated circuit, which could be re-configured the logic function.

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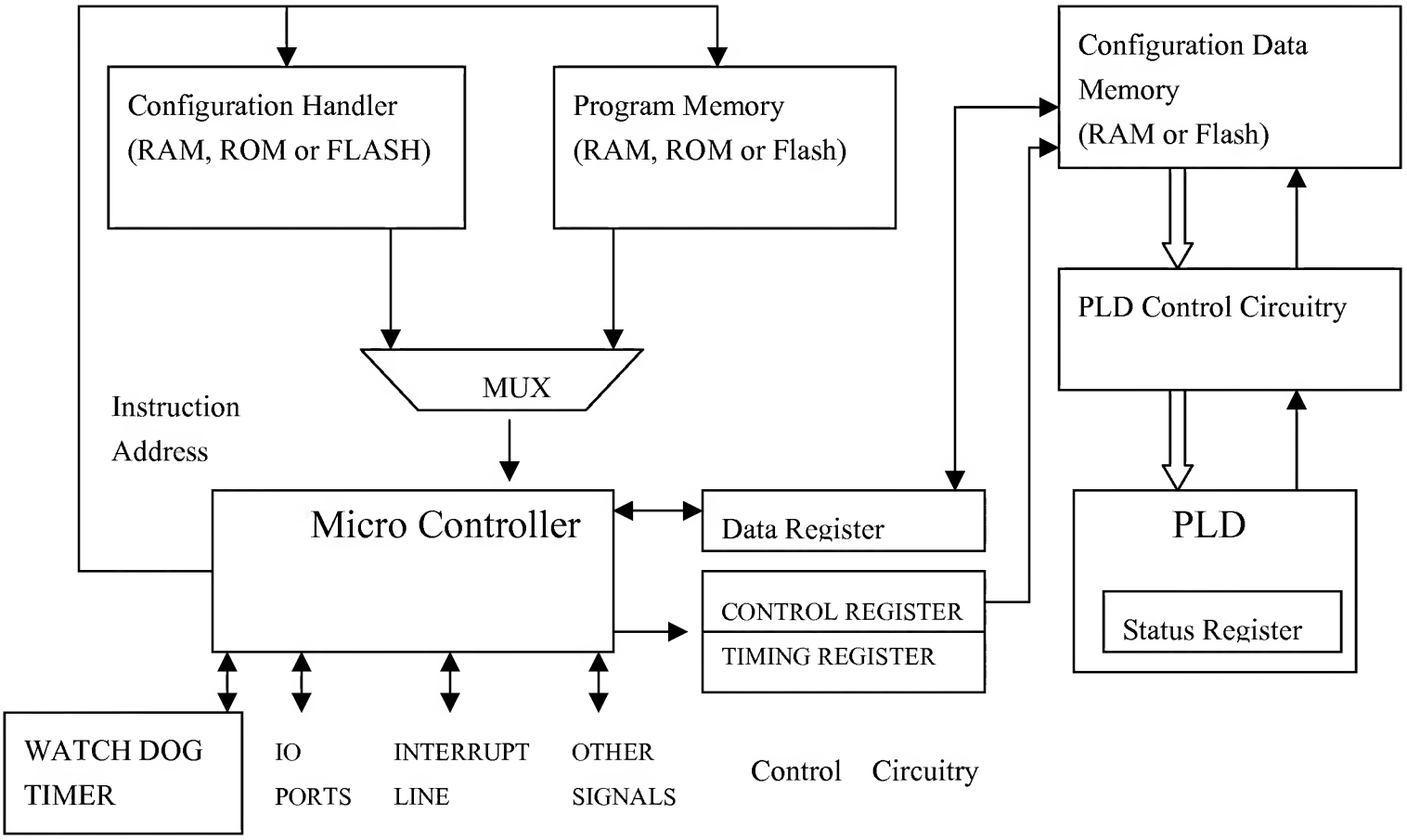
INVENTION DISCLOSURE FORM

(專利提案揭露書)

(Please fill out this form following the instructions in English or Chinese)

8. Showing related drawings or experimental data about this invention.
(示出本發明相關之圖式或實驗數據)



9. Witnesses : This Invention Disclosure Form consisting of ___ pages has been read and understood by
(見證人已詳讀本專利提案揭露書共 ___ 頁，並確實瞭解記載內容)

First Witness (第一人)		Second Witness (第二人)	
Signature (簽名)	Date (日期)	Signature (簽名)	Date (日期)

（如需增頁，請自行複製本空白表單，並確定每頁均簽上姓名及日期）

發明人簽名：_____ _____ _____ _____ _____

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